**Amendments To The Claims**

The following list of the claims replaces all prior versions and lists of the claims in this application.

Claims 1-27 (Canceled).

28. (Currently amended) At least one high-k device, comprising:

a structure having a strained substrate formed thereover, the strained substrate comprising an uppermost strained-Si epi layer, a middle relaxed $Si_{1-x}Ge_x$ layer and a lowermost graded $Si_{1-y}$ $Ge_y$ layer, the uppermost strained-Si epi layer being disposed directly on the middle relaxed $Si_{1-x}Ge_x$ layer;

at least one dielectric gate oxide portion over the strained substrate, the at least one dielectric gate oxide portion having a dielectric constant of greater than about 4.0; and

a device over each of the at least one dielectric gate oxide portion to complete the at least one high-k device.

29. (Previously presented) The device of claim 28, the uppermost strained-Si epi layer having a thickness of from about 100 to 500Å; the middle relaxed $Si_{1-x}Ge_x$ layer having a thickness of from about 1000 to 50,000Å; and the lowermost graded $Si_{1-y}$ $Ge_y$ layer having a thickness of from about 200 to 50,000Å.

30. (Previously presented) The device of claim 28, where x is greater than 0 and less than about 0.50 and where y is 0 or about 0 proximate the structure and increases to about x proximate the middle relaxed $Si_{1-x}Ge_x$ layer, wherein $x \geq y$.

31. (Previously presented) At least one high-k device, comprising:

a structure having a strained substrate formed thereover, the strained substrate comprising an uppermost strained-Si epi layer, a middle $Si_{1-x}Ge_x$ layer and a lower silicon oxide layer;

at least one dielectric gate oxide portion over the strained substrate, the at least one dielectric gate oxide portion having a dielectric constant of greater than about 4.0; and

a device over each of the at least one dielectric gate oxide portion to complete the at least one high-k device.

32. (Previously presented) The device of claim 31, wherein the uppermost strained-Si epi layer has a thickness of from about 100 to 500Å, the middle $Si_{1-x}Ge_x$ layer has a thickness of from about 700 to 1200Å and the lower silicon oxide layer has a thickness of from about 800 to 2000Å.

33. (Previously presented) At least one high-k device, comprising:

a structure having a strained substrate formed thereover, the strained substrate comprising an uppermost strained-Si epi layer over an upper relaxed $Si_{1-x}Ge_x$ layer over a graded $Si_{1-y}$ $Ge_y$ layer over an epi layer over a lowermost relaxed $Si_{1-z}$ $Ge_z$ layer, wherein $x \geq y \geq z$;

at least one dielectric gate oxide portion over the strained substrate, the at least one dielectric gate oxide portion having a dielectric constant of greater than about 4.0; and

a device over each of the at least one dielectric gate oxide portion to complete the at least one high-k device.

34. (Previously presented) The device of claim 33, the uppermost strained-Si epi layer having a thickness of from about 100 to 500Å; the upper relaxed $Si_{1-x}Ge_x$ layer having a thickness of from about 1000 to 50,000Å; the graded $Si_{1-y}$ $Ge_y$ layer having a thickness of from about 2000 to 50,000Å; the epi layer having a thickness of from about

20 to 500Å; and the lowermost relaxed $Si_{1-z}$ $Ge_z$ layer having a thickness of from about 200 to 50,000 Å.

35. (Previously presented) The device of claim 33, the uppermost strained-Si epi layer having a thickness of from about 150 to 300Å; the upper relaxed $Si_{1-x}Ge_x$ layer having a thickness of from about 2000 to 40,000Å; the graded $Si_{1-y}$ $Ge_y$ layer having a thickness of from about 500 to 25,000Å; the epi layer having a thickness of from about 50 to 200Å; and the lowermost relaxed $Si_{1-z}$ $Ge_z$ layer having a thickness of from about 500 to 25,000Å.

36. (Previously presented) The device of claim 33, where x is no less than y and less than about 0.50, where y is no less than z proximate the epi layer and increases to about x proximate the upper relaxed $Si_{1-x}Ge_x$ layer, and where z is greater than 0 and less than about 0.50.

37. (Previously presented) The device of claim 33, wherein the at least one dielectric gate oxide portion being comprised of $HfO_2$ or $HfSiO_4$.

38. (Previously presented) The device of claim 41, wherein the relaxed $Si_{1-y}$ $Ge_y$ layer has a thickness of from about 200 to 30,000Å, the constant $Si_{1-y}$ $Ge_y$ layer has a thickness of from about 200 to 20,000Å, the silicon epi layer has a thickness of from about 20 to 500Å, the constant $Si_{1-z}$ $Ge_z$ layer has a thickness of from about 200 to 20,000Å, and the uppermost strained-Si epi layer has a thickness of from about 20 to 500Å.

39. (Previously presented) The device of claim 41, wherein the relaxed $Si_{1-y}$ $Ge_y$ layer has a thickness of from about 300 to 5000Å, the constant $Si_{1-y}$ $Ge_y$ layer has a

thickness of from about 300 to 5000Å, the silicon epi layer has a thickness of from about 50 to 300Å, the constant $Si_{1-z}$ $Ge_z$ layer has a thickness of from about 300 to 5000Å, and the uppermost strained-Si epi layer has a thickness of from about 50 to 300Å.

40. (Previously presented) The device of claim 41, wherein the at least one dielectric gate oxide portion is comprised of $HfO_2$ or $HfSiO_4$.

41. (Previously presented) At least one high-k device, comprising:

a structure having a strained substrate formed thereover, the strained substrate comprising an uppermost strained-Si epi layer, a relaxed $Si_{1-y}$ $Ge_y$ layer under the uppermost strained-Si epi layer, a constant $Si_{1-y}$ $Ge_y$ layer under the relaxed $Si_{1-y}$ $Ge_y$ layer, a silicon epi layer under the constant $Si_{1-y}$ $Ge_y$ layer, and a constant $Si_{1-z}$ $Ge_z$ layer under the silicon epi layer, wherein the uppermost relaxed-Si epi layer is comprised of $Si_{1-x}$ $Ge_x$ wherein x is constant or graded;

at least one dielectric gate oxide portion over the strained substrate, the at least one dielectric gate oxide portion having a dielectric constant of greater than about 4.0; and

a device over each of the at least one dielectric gate oxide portion to complete the at least one high-k device.

42. (Previously presented) At least one high-k device, comprising:

a structure having a strained substrate formed thereover, the strained substrate comprising at least an uppermost strained-Si epi layer having a dislocation density of strained-Si epi of less than about $1E6/cm^2$;

at least one dielectric gate oxide portion over the strained substrate, the at least one dielectric gate oxide portion having a dielectric constant of greater than about 4.0; and

a device over each of the at least one dielectric gate oxide portion to complete the at least one high-k device.

43. (Previously presented) The structure of claim 42, wherein the at least one dielectric gate oxide portion is comprised of $Hf0_2$, $HfSi0_4$, N-doped hafnium. $HfSiO_X$, $ZrO_2$, $ZrSiO_X$ or N-doped zirconium silicate.

44. (Previously presented) The device of claim 42, wherein the structure is a silicon substrate or a germanium substrate.

45. (Previously presented) The device of claim 42, wherein the strained substrate is comprised of only the uppermost strained-Si epi layer.

46. (Previously presented) At least one high-k device, comprising:

a structure having a strained substrate formed thereover, the strained substrate comprising only an uppermost strained-Si epi layer having a thickness of from about 100 to 500Å;

at least one dielectric gate oxide portion over the strained substrate, the at least one dielectric gate oxide portion having a dielectric constant of greater than about 4.0; and

a device over each of the at least one dielectric gate oxide portion to complete the at least one high-k device.

47. (Previously presented) The device of claim 46, the uppermost strained-Si epi layer having a thickness of from about 150 to 300Å.

48. (Previously presented) The device of claim 46, the uppermost strained-Si epi layer having a thickness of from about 200 to 300Å.